AMENDMENT

IN THE SPECIFICATION:

Please amend the specification by replacing the paragraph on page 8, line 14 with the following:

--**Figure 18A-18E**   Faceplate covers--

IN THE ABSTRACT:

Please include the following abstract at the end of the Specification and Claims:

--*Abstract of the Invention*

A controller for executing an application program to process control information related to control elements includes one or more main processors that each run the application program; a time synchronization system that synchronizes the time clocks of the main processors; and a voting system that exchanges information between the main processors and compares the information received from the other main processors. In addition, the controller includes one or more rendezvous signals sent to and received by the main processors as well as a mechanism for updating the time clocks based on a clocking midpoint of all processor signals.--

IN THE CLAIMS:

Please cancel claims 17-20, 39-43, 45, 48-49, 55, 57, 63-64, 66-68, 74, 100, 101, 104, 105, and 107 without prejudice or disclaimer of the subject matter contained therein.

Please amend claims 1, 6, 7, 11-13, 16, 21-22, 28-29, 32-35, 50-53, 69, 71, 77, and 93-94 in the following manner. The amendments to these claims are indicated in the attached Appendix.

1.   (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to said control elements, communicating with each main processor module;

at least one communication module communicating external signals to said plurality of main processor modules;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of main processor modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint;

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint; and

a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors.

6.   (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to said control elements communicating with each main processor module;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of main processor modules and compares the information

in each selected main processor module with the information in other selected ones of said main processor modules;

a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint.

7.   (Twice Amended) A controller as described in claim 6 wherein there are a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors and wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, and other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module.

11.   (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to control elements, communicating with each main processor module;

at least one communication module communicating external signals to said plurality of main processor modules;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint.

12.   (Twice Amended) A controller as described in claim 11 wherein there are a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors and wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

13.   (Twice Amended) A controller as described in claim 11 wherein there are a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors and wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

16.   (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

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21.   (Twice Amended) A controller for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

22. (Twice Amended) A controller as described in claim 21 wherein there are a plurality of base plate circuit boards receiving said housing for said main processor modules.

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28. (Twice Amended) A controller as described in claim 21 further comprising:

at least one input/output module for receiving and sending control information to control elements in said control system communicating with each of said plurality of main processor modules; and

at least one communication module for sending and receiving external signals communicating with each of said plurality of main processor modules.

29. (Twice Amended) A control system platform for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

at least one communication module communicating external signals to said plurality of main processor modules;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

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32. (Twice Amended) A control system platform as described in claim *27* wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

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33. (Twice Amended) A control system platform as described in claim *27* further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

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34. (Twice Amended) A control system platform for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors;

a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

35. (Twice Amended) A control system platform as described in claim 34 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, and other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module.

50. (Twice Amended) A computer control system for executing an application program to process control information related to control elements comprising:

a plurality of main processor modules each of which runs the application program;

at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

a time synchronizing system for synchronizing the time clocks of said main processor modules;

a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

a selection system which determines which of said plurality of main processor modules is a selected main processor module which is used to compare information in each main processor module;

a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards;

a common rail system for mounting of said housings and providing electronic connections to each of said housings;
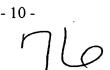
apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules;

a system for determining the clocking midpoint of all processor signals;

a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint.

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5%. (Twice Amended) A control system platform for executing a control system program for managing a control system and evaluating the accuracy of information related to said control system, said platform comprising:

a plurality of main processor modules, each executing a copy of said application program;

at least one field input/output module communicating with each main processor module;

a voting system for comparing information between said main processor modules, and

a restoring system for restoring valid information for access by said main processor modules;

apparatus for sending a rendezvous signal to all other main processor modules;

apparatus for receiving a rendezvous signal from all other main processor modules; and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

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~~52~~. (Twice Amended) A control system platform as described in claim ~~51~~ *37* wherein said information is selected from the group consisting of:

program code,

fault detection information,

sensor information,

command information,

output information, and

input information.

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~~53~~. (Twice Amended) A control system for executing an application program and evaluating the accuracy of input/output information comprising:

a plurality of main processor modules, each executing said application program;
at least one field input/output module communicating with each main processor module;

a voting system for comparing information between said main processor modules; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including:

apparatus for sending a rendezvous signal to all other main processor modules,

apparatus for receiving a rendezvous signal from all other main processor modules, and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

40. (Twice Amended) A voting system which exchanges information between selected ones of a main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules comprising:

an apparatus for loading control system related information from each processor for storage in every other processor;

a comparison apparatus for comparing loaded control system related information with the comparing processor's control system information;

memory for storing the results of said comparison;

a selection apparatus for determining which loaded information compares with said comparing processor's information;

a default apparatus for storing a default indication where the comparing processor's information fails to compare with a majority of said loaded processor information; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including:

apparatus for sending a rendezvous signal to all other main processor modules,

apparatus for receiving a rendezvous signal from all other main processor modules, and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

41. (Twice Amended) A control system for executing an application program and evaluating the accuracy of input/output information comprising:

a plurality of main processor modules;

at least one field input/output module communicating with each main processor module;

a voting system for comparing information between said main processor modules; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including:

apparatus for sending and receiving rendezvous signals to and from all other main processor modules, and

a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

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77. (Twice Amended) A control system platform for running a control system program which processes information related to a control system; said control system platform comprising:

a plurality of processors executing said control system program and processing said control system information said processors mounted to a common power rail;

at least one input/output module for sending and receiving said information related to said control system; communicating with each of said processors mounted to said common power rail communicating with said plurality of processors;

at least one communication module for receiving external signals and exchanging external signals with each of said processors and external signals; mounted to said common power rail communicating with said plurality of processors over a communications bus;

a validation system on each processor for evaluating said control system information to be processed by said control system program prior to processing by said control system program; said evaluation system comparing categories of information stored in memory on each processor with the same category of information in memory on other processors and selecting information on which a majority of processors compare as valid information and storing said valid information into the memory of any processor for which the information did not compare with the majority of processors;

each of said processors being interconnected on an inter-processor bus through a loop-back path; said loop back path applying the signals for transmitting information by each

transmitting processor to other processors on said bus as an attenuated loop-back signal to said transmitting processor;

a storage area in the transmitting processor memory for storing said loop-back information;

a comparator for comparing signals transmitted by said other processors on said bus with said loop back signals to determine if the information in said loop-back signals is the same as the signals transmitted by said other processors; and

a time synchronizing system for synchronizing the time clocks of said main processor modules including apparatus for sending and receiving rendezvous signals to and from all other main processor modules and a clock update apparatus which sends update signals to the clock based on the clocking midpoint of all processor signals.

43. (Twice Amended) A method for determining the voting mode of a plurality of processors each having memory and coupled to a inter processor bus comprising the steps of:

exchanging information with said plurality of processors over said bus transmitting a category of information from a first processor on said bus to a second processor on the bus;

passing said transmitted information through an attenuated loop-back path to said first processor;

capturing said transmitted loop-back information in said first processor memory;

comparing said attenuated loop back information captured in said first processor memory with the information transmitted by said first processor;

storing a first result of said comparing in said first processor's memory;

faulting the first processor when the first result indicates a difference in said information;

capturing second processor information which is received by said first processor from a second processor on said bus in said first processor memory;

comparing said second processor captured information with the same category of information in said first processor;

faulting the second processor when the second result indicates a difference in said information;